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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,774	09/17/2003	Kyoung Mook Lee	8733.915.00-US	1766

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EXAMINER	
NGUYEN, DUNG T	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/663,774	LEE ET AL.	
	Examiner	Art Unit	
	Dung Nguyen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/07/2005 has been entered.

2. Applicant's amendment dated 12/07/2005 has been received and entered. By the amendment, claims 1-30 are currently pending in the application.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a second gate redundancy line, a second gate contact hole must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the limitation of "the second gate redundancy line electrically connected with the first gate redundancy line through a second gate contact hole" is not disclosed in the specification.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 8, 14 and 20, it is confusing and unclear how a first gate redundancy line can be *electrically* connected with *just* one of the gate electrode, the gate line (emphasis added).

Correction to the claimed language is suggested to clarify the claimed subject matter.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, 7-19 and 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al., US Patent No. 6,215,541, in view of Ozaki et al., US Patent No. 6,184,947.

Regarding claims 1 and 8, Song et al. disclose an array substrate for a liquid crystal display (LCD) device (Fig. 5) a substrate (100), a gate line (20) and a thin film transistor having a gate electrode (21), a source electrode (61), a drain electrode (62) and an active Layer (40) formed over the substrate (100), an interlayer insulating layer (30) formed on the thin film transistor, a first gate redundancy line (fig. 5, 82) formed on the interlayer insulating layer, and connected electrically with one of the gate electrode (21), the gate line (20), and both the gate electrode (20) and gate line (20) through a first gate contact hole (72). Song also discloses a passivation layer (70) provided on the first gate redundancy line and the interlayer insulating layer (30) and a pixel electrode (66) electrically connected with the drain electrode through the

drain contact hole formed in the passivation layer (fig. 17b). Song teaches that the gate redundancy line is made of chromium, molybdenum or molybdenum alloy.

Song et al. , however, do not teach that the gate redundancy line is formed of the same material as one of the source and drain electrodes, which are made from a semiconductor material as, can be seen from Fig. 7. Ozaki in disclosing thin film transistor matrix with repair bus lines teaches that the gate line (GL) can also be made of a semiconductor layer having a high impurity concentration (col. 3, lines 62-64). Therefore, it would have been obvious to one having ordinary skill in the art at
the time the invention was made to adapt the gate line made from a semiconductor material (as taught by Ozaki) in place of metals such as chromium, molybdenum or molybdenum alloy (as taught by Song) to avoid pin holes that might be formed in the
metal layers and to repair any breakage in the metal layer (col. 2, lines 49-56).

Regarding claims 2-5, 7 and 9-13, Song et al. teach the thin film transistor as a bottom gate thin film transistor, the first gate contact hole (75) is formed passing through the interlayer insulating layers and also teaches a second gate contact hole for connection of the first gate redundancy line with the gate line (Fig. 5) and (col. 6, lines 1-9). Ozaki teaches that the thin film transistor can also be a top gate thin film transistor (Fig. 1 D).

Regarding claims 14 and 24, Song et al. disclose the method of fabricating the array substrate for a liquid crystal display in (col. 11 , lines 13-67), (col. 12, lines 1-67) and (col. 1 3jlines 1-10). The method comprises forming a gate line and a gate electrode on a substrate, forming an interlayer insulating layer on the gate line and the gate electrode, forming a thin film

transistor with the gate electrode, a source electrode, a drain electrode, and an active layer, forming a first gate redundancy line on the

interlayer insulating layer electrically connected with one of the gate electrode, the gate line, and both the gate electrode and gate line through a first gate contact hole, forming a passivation layer on the first gate redundancy line and the interlayer insulating layer, and forming a drain contact hole in the passivation layer, and forming a pixel electrode connected electrically with the drain electrode through the drain contact hole.

Regarding claims 15-19, 23 and 25-30, Song et al. disclose the array substrate for the LCD as recited above where the formation of the thin film transistor is as a bottom gate thin film transistor, the first gate contact hole (72) is formed passing through the interlayer insulating layers and also teaches a second gate contact hole for connection of the first gate redundancy line with the gate line (Fig. 5) and (col. 6, lines 1-9). Ozaki teaches that the formation of the thin film transistor as a top gate thin film transistor (Fig. 1D).

9. Claims 6 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al., US Patent No. 6,184,947, in view of Ozaki as applied to claims 1 and 14 above, and further in view of Huh et al., U.S Patent No. 6,307,216.

Regarding the above claims, the modification to the Song et al. discloses the array substrate for LCD as recited above, however, neither reference teaches the formation of a second gate line. Huh et al. in disclosing a thin film transistor panel for liquid crystal displays, teaches the use of a second gate line and electrical connection to the first gate line (col. 2, lines 26-43) and (col. 3, lines 45-67). Huh et al. also teaches the contact holes (C1 , C2 and C3) formed in the passivation film (30) and the material of the connect pattern is made of the same material as the

pixel electrode (col. 4, lines 23-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the second gate line and its electrical connection to the first gate line as disclosed by Huh to the devise of Song in view of Ozaki to provide a redundancy line structure used for effectively repair disconnection defects without introducing additional steps and for preventing short-circuited defects between the upper and the lower substrates and between adjacent pixels (col. 1, lines 45-55).

Response to Arguments

10. Applicant's arguments filed 12/07/2005 have been fully considered but they are not persuasive.

Applicant contends that Song fails to teach or suggest the gate redundancy line is connected electrically with just one of the gate electrode, the gate line, and both the gate electrode and gate line through the gate contact hole (amendment, page 8). The Examiner is not convinced by this argument since the same is true of the Song's gate redundancy line (82) as stated above. It should be noted that, as stated above, the term of "just" is not a proper term to use in connect with the "electrically connection". In other words, the Applicant's gate redundancy line and the Song's gate redundancy line would be the same as well.

Accordingly, the limitation of the above claims met.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung Nguyen whose telephone number is 571-272-2297. The examiner can normally be reached on Tuesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DN
03/06/2006

Dung Nguyen
Primary Examiner
Art Unit 2871